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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/091,783	03/06/2002	Karthik Balakrishnan	004-5827	8975

22120 7590 09/24/2004

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EXAMINER	
COLEMAN, ERIC	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 09/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/091,783	BALAKRISHNAN ET AL.	
	Examiner	Art Unit	
	Eric Coleman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-56* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17,21,23-29,and 35-51* is/are rejected.

7)☒ Claim(s) *18-20,22,30-34 and 52-56* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-4,6-12,23,24,26-28,35-38,40-44,45,46 are rejected under 35 U.S.C. 102(b) as being anticipated by Murray (patent No. 5,142,631).

3. Murray taught the invention as claimed including a data processing ("DP") system comprising:

a) Generating a first plurality of select masks for a first plurality of instructions immediately preceding a group of instructions (e.g., see fig.4, and col. 10, lines 63-col. 12, line 14); and

b) Selecting a second plurality of select masks from the first plurality of select masks using a write pointer figs. 5,6 and col. 12, lines 15-col. 14, line 51).

4. As per claims 2,36, Murray taught fetching the group of instructions (e.g., see figs. 1,2 and col. 7, line 46-col. 8, line 27, and col. 9, line 29-col. 10, line 25).

5. As per claims 3,37 Murray taught the write pointer identifies a current instruction from the group of instructions (e.g., see col. 11, lines 20-22, and col. 12, lines 15-60);

6. As per claims 4,6, 7,8,10, 24,38,40,41,42,44 Murray taught the group of bits comprising a mask being 8 bits for 8 registers or 16 for 16 registers or 32 for 32 registers or 64 bits for 64 registers or 128 for 128 registers (e.g., see col. 11, lines 2-37).

Since the each register bit is set because an instruction was to executed that accessed the particular register then the Murray system performs a method that provides for the storing and processing register data for tracking dependencies of groups of instructions corresponding to the number of registers (e.g., 8, or 16 or 32 or 64 or 128).

7. As to claim 9,11,12, 23,43,45,46 Murray taught different sizes of the group of instructions being tracked from a low of 8 to a high of 128 (e.g., see col. 11, lines 2-37). Clearly the it would have been inherent in the processing of instruction dependencies where only 8 instructions were tracked the performance would have had to have been faster than the performance of the implementation when a substantially larger number of instructions were tracked (e.g., 128). Therefore Murray taught implementations with a fast scoreboard and with a slow scoreboard.

8. As per claim 26,27,28 Murray taught an instruction picker (25) for selecting an instruction for execution (e.g., see fig. 3, and col. 9, lines 3-25) that does not have the dependencies (e.g., see fig.8 and col. 8, line 18-col. 10, line 20) coupled to the dependency scoreboard (e.g., see fig. 3) which comprises a slow dependency when the implementation uses the large scoreboard (e.g., 128 bit) with 128 registers (e.g., see col. 11, lines 2-37).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 5,13,14,16,17,39,47,48,50,51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murray (patent No. 5,142,631).

11. Murray taught the invention as substantially as claimed including a data processing ("DP") system comprising:

a) Generating a first plurality of select masks for a first plurality of instructions immediately preceding a group of instructions (e.g., see fig.4, and col. 10, lines 63-col. 12, line 14); and

b) Selecting a second plurality of select masks from the first plurality of select masks using a write pointer figs. 5,6 and col. 12, lines 15-col. 14, line 51).

12. As per claim 2, Murray taught fetching the group of instructions (e.g., see figs. 1,2 and col. 7, line 46-col. 8, line 27 and col. 9, line 29-col. 10, line 25).

13. As per claim 3, Murray taught the write pointer identifies a current instruction from the group of instructions (e.g., see col. 11, lines 20-22 and col. 12, lines 15-60);

14. As per claims 4,6, 7,8,10 Murray taught the group of bits comprising a mask being 8 bits for 8 registers or 16 for 16 registers or 32 for 32 registers or 64 bits for 64 registers or 128 for 128 registers (e.g., see col. 11, lines 2-37). Since the each register bit is set because an instruction was to executed that accessed the particular register then the Murray system performs a method that provides for the storing and processing register data for tracking dependencies of groups of instructions corresponding to the number of registers (e.g., 8, or 16 or 32 or 64 or 128).

15. As to claim 9,11,12 Murray taught different sizes of the group of instructions being tracked from a low of 8 to a high of 128 (e.g., see col. 11, lines 2-37). Clearly the it would have been inherent in the processing of instruction dependencies where only 8 instructions were tracked the performance would have had to have been faster than the performance of the implementation when a substantially larger number of instructions were tracked (e.g., 128). Therefore Murray taught implementations with a fast scoreboard and with a slow scoreboard.

16. As per claims 5,13,39,47 Murray taught auto-increment and auto-decrement addressing modes for automatically stepping a register though elements of a table or array (e.g., see col. 3, lines 4-36) where the register is incremented or decremented by 1,2,,4 or 8 depending whether the operand is 1,2,4, or 8 bytes in length in the scoreboard (e.g., see col. 11, lines 30-37). Here one of ordinary skill would have been motivated to mod eight rotate the instruction at least to access the each next instruction for processing especially when the instructions were 8 bits (1 byte) in length and the scoreboard would have been organized in octets.

17. As to claim 14,48 Murray taught a scoreboard that comprises at least a single strand of instructions (e.g., see figs 1 and col. 6, lines 27-68).

18. As per claim 16,17,50,51 Murray taught decoders generating the select masks. Therefore since decoding functions are characteristically generated using truth tables then one of ordinary skill would have been motivated to use truth tables in the generation of the select masks. Also, since Murray taught an implementation with 1-byte

instructions therefore one of ordinary skill would have been motivated to enable the truth table to identify a select mask for a first instruction of each of each of the octet.

19. Claims 15,21,25,29,49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murray as applied to claims 1-14,23,26,35,47 above, and further in view of Leung (patent No. 5,790,827).

20. Leung taught (claims 15,49) a system with plural scoreboard scoreboards hierarchically coupled and comprising single and double precision registers use for processing of plural instruction strands (integer and floating point strands)(e.g., see col. 9, lines 24-65).

21. As per claim 25, Leung taught plural smaller sized scoreboards (faster scoreboards) and a larger main scoreboard (slow scoreboard) (e.g., see figs. 4,6, and col. 9, line 24-col. 12, line 61).

22. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Murray and Leung. One of ordinary skill would have been motivated to incorporate the Leung teachings of multiple scoreboards into the Murray system at least to provide a more efficient and quicker determination of dependencies (e.g., see col., 3 lines 3-35, and col. 12, lines 25-50 of Leung).

23. Murray taught (claim 21) selecting a first group of dependencies from the dependencies using the second plurality of select masks (figs. 5,6 and col. 12, lines 15-col. 14, line 51). Murray taught different sizes of the group of instructions being tracked from a low of 8 to a high of 128 (e.g., see col. 11, lines 2-37).

24. As per claim 29, Leung taught a system for concurrent execution of instructions by plural execution units (e.g., see col. 6 line 4-col. 8, line 58).

Allowable Subject Matter

25. Claims 18-20,22,30-33,34,52-56 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Liebholz (patent No. 6,122,728) disclosed a technique for ordering internal processor register accesses (e.g., see abstract).

Nataraj (patent No. 6,757,779) disclosed a content addressable memory with selectable mask write mode (e.g., see abstract).

Narayan (patent No. 5,781,789) disclosed a superscalar microprocessor employing parallel mask decoder (e.g., see abstract).

Edmondson (patent No. 5,471,591) disclosed a combined write-operand queue and read-after-write dependency scoreboard (e.g., see abstract) and taught that prior art reference (patent No. 5,142,631)(the Murray reference cited above) specifically comprised register scoreboard queue with logical Oring of source masks (e.g., see col. 3, lines 35-63).

Budde (patent No. 4,891,753) disclosed a system with register scoreboarding on a microprocessor chip (e.g., see abstract)

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (703) 305-9674 or (571) 272-4163. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EC

ERIC COLEMAN
PRIMARY EXAMINER